REMARKS

This paper responds to the Office Action mailed June 12, 1998 ("the Office Action"). Applicant respectfully requests reconsideration of the present application in light of the above amendments and the following remarks.

35 U.S.C. § 112

Section 1 of the Office Action rejected claims 1, 8, 13 and 15 under 35 USC 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The particular section 112 issues raised in the Office Action are addressed in turn below.

Level conversion.

The Office Action alleges that the claims are incomplete and lack recitation of critical features of the invention, and states that, in the independent claims of the present invention, "the recitation that the circuit and/or method performs level conversion does not appear to be supported by the claimed invention." The Applicant respectfully traverses this rejection.

The structure and/or method claimed in each of the independent claims of the present application does perform level conversion. The Office Action contends that the inverter, and not the elements recited in the independent claims, performs the level conversion function. However, in an exemplary embodiment of the present invention, wherein the buffer comprises an inverter, the inverter performs an inversion function -- converting a logically high signal to a logically low signal, or vice versa. The elements claimed in the independent claims convert signals of a first voltage level to a second voltage level.

For instance, independent claim 1 includes the elements of a transistor, a capacitor coupled across the input and output terminals of the transistor, and a resistive element having a first end portion coupled to a voltage supply. Referring now to the above listed elements of independent claim 1 in conjunction with the exemplary embodiment illustrated in Fig. 1 of the present application, the input terminal 12 of the transistor 16 is connected to an input signal that is digital in nature and can vary, for example, between about 0 and 2.5 volts. Thus, when a logically high signal (about 2.5 volts) is present at the input terminal (drain) 12 of the transistor 16, the output terminal (source) of the transistor 16, or node A, will charge toward a voltage level of about V_{bias} - V_{tn}, where V_{tn} is the threshold voltage of the transistor 16. Hence, the elements recited convert a signal of a first preselected level to a second preselected level (about 2.5 volts and about 1.8 volts - V_{tn}, respectively, in the embodiment of Fig. 1).

Therefore, the Applicant respectfully submits that the rejection regarding the lack of critical features of the invention is improper, and should thus be withdrawn.

Parasitic capacitance and "pump"

The Office Action next alleges that independent claim 8 improperly recites an effect of the other claim elements, i.e. "parasitic capacitance," as one of the elements of the invention. Further, the Office Action contends that the claim language reciting a pump is misdescriptive. The Applicant respectfully traverses these rejections.

Among other things, independent claim 8 includes the elements of a capacitor coupled between the source and drain of a pass gate transistor, and a pump coupled to the gate of the pass gate transistor. The pump temporarily increases the voltage level applied to the gate of the pass gate transistor. It appears that the Office Action contains a misinterpretation of the claim language.

Referring again to the circuit diagrams of Figs. 1 and 2 in the present application, illustrating exemplary embodiments in accordance with the present invention, the pass gate transistor 16 has a capacitor 22 coupled thereacross. In the embodiment illustrated in Fig. 2, the capacitor 22 comprises a PMOS transistor with its gate coupled to node A and its source, drain and substrate coupled to the input terminal 12. The AC bypass capacitor 22 enhances the transition time of the voltage appearing at node A in response to a corresponding transition in a signal applied to the input terminal 12. Thus, the "capacitor" element of claim 8 is not simply an effect of the other elements of the claim.

In one embodiment in accordance with the invention, the pump element of claim 8 comprises a resistor coupled between the gate of the pass gate transistor and the voltage supply, and a capacitor coupled to the gate of the pass gate transistor to receive the input signal. Such embodiments are claimed, for example, in claims 9 -12 of the present application. In the exemplary embodiments illustrated in Figs. 1 and 2 of the present application, the pump includes a resistor 18 coupled between the voltage supply V_{bias} and the gate (node B) of the pass gate transistor 16, and a parasitic capacitor 20 located between the input terminal 12 and node B, which operate to temporarily increase the voltage applied to the gate of the pass gate transistor 16 during a low to high transition at the input terminal 12.

Referring now to the particular embodiment of the invention illustrated in Fig. 2 of the present application, the resistor comprises a PMOS transistor 30, and the capacitor comprises a parasitic capacitor 20. The PMOS transistor 30 is coupled between V_{bias} and the gate of the pass gate transistor 16 (node B), and the parasitic capacitor 20 is coupled between the input terminal 12 and node B. Assuming V_{bias} is about 1.8 volts, and the signal at the input terminal 12 varies

between logically low and high levels of about 0 and 2.5 volts, respectively, the voltage at the gate of the pass gate transistor 16 is about 1.8 volts prior to an input signal transition from a logically low level to a logically high level. Since the voltage across the capacitor 20 cannot change instantaneously with the change in the input voltage level, the voltage level at the gate of the pass gate transistor 16 is pumped up toward the voltage level $V_{bias} + \alpha V_{in}$ (where $\alpha < 1$). Thus, the voltage level applied to the gate of the pass gate transistor 16 (node B) is temporarily increased, biasing the pass gate transistor 16 "on" harder, thereby causing the voltage at node A to rise at a faster rate than would otherwise occur than without the presence of the resistor 18.

For these reasons, the Applicant respectfully submits that the recitation of a capacitor and a pump in claim 8 is proper, and that claim 8, and the claims depending therefrom, are in allowable form.

"Adapted" language

Finally, section 1 of the Office Action alleges that the use of the language "adapted to" is indefinite. In an effort to move the present application towards allowance, the claims have been amended to remove the phrase "adapted to" to further clarify the claim language. The amendments presented herein above are solely for the purpose of clarifying the claim language in light of the 35 USC 112 rejection, and not for the purpose of overcoming prior art rejections.

In light of the above amendments and remarks, the Applicant respectfully submits that the 35 USC 112 rejections are overcome, and the all of the pending claims of the present application are in proper form for allowance.

Objection to the disclosure

Section 2 of the Office Action objected to the disclosure because of informalities. The Examiner's careful consideration of the claims is appreciated. Claim 1 has been amended to correct the informality; therefore, the Applicant believes that the objection to the disclosure has been overcome.

35 U.S.C. § 103

Section 3 of the Office Action rejected claims 1-16 under 35 USC 103(a) as being unpatentable over U.S. Patent No. 4,636,907 to Howell ("Howell") or U.S. Patent No. 4,688,267 to Chown et al. ("Chown"). The Applicant respectfully traverses these rejections.

The Office Action, in section 3, admits that Howell and Chown simply disclose an input signal being applied to an inverter through a resistive load. The Office Action further admits, in section 2 regarding the section 112 rejections, that the independent claims of the present application do not include the element of an inverter. In light of the remarks presented herein above, it appears that the present invention is clearly patentable over either Howell or Chown.

Howell is directed to an arcless circuit interrupter. The circuit interrupter disclosed in Howell does not convert signals of a first preselected level to a second preselected voltage. Thus, the application of Howell as prior art to the present application does not appear to be proper. Similarly, Chown is directed to an optical fibre receiver, and therefore, also does not appear to be analogous prior art.

Further, neither Howell nor Chown teach or suggest all of the elements of the independent claims of the present application. For instance, nowhere in Howell or Chown is

there a disclosure or suggestion of a transistor having an input terminal that receives signals of a first preselected voltage level and an output terminal that delivers signals of a second preselected voltage level. Nor do Howell or Chown teach or suggest a pump element coupled to the gate of a pass gate transistor to temporarily increase the voltage level applied to the gate, or any means for temporarily increasing the voltage level applied to the gate..

Moreover, Howell and Chown do not disclose a method for converting an input signal of a first preselected voltage level to a second preselected voltage level, and particularly, neither Howell nor Chown teach or suggest the steps of charging the gate of a pass gate transistor to a third voltage level to enable the pass gate transistor to pass at least a portion of the voltage level of the input signal to an output node; charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time, said fourth preselected voltage level being greater than said third preselected level; and passing at least a portion of any AC component in said input signal to said output node.

Therefore, the Applicant respectfully submits that the claims of the present application are patentable over both Howell and Chown.

Conclusion

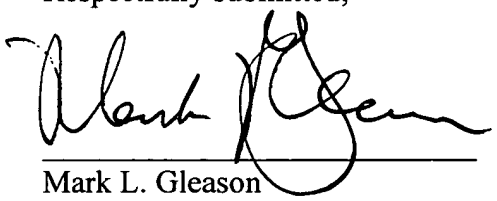
Based upon the above amendments and remarks, Applicant believes that the pending claims are in proper form for allowance. Therefore, reconsideration of these claims is respectfully requested.

If the Examiner believes that a telephone conference would be beneficial to advance this case towards allowance, he is strongly encouraged to telephone the undersigned at the number provided below.

The date for response to the Office Action, in accordance with the three-month shortened statutory period for response, was September 12, 1998, which fell on a Saturday. Thus, the response date is extended to, and includes, September 14, 1998. Therefore, no fee is believed due for the consideration of this response, or any of the amendments or information presented herein. If, however, a fee is necessary, the Commissioner is authorized to charge any such fee to Account No. 01-2508/INPA:035/GLE.

Respectfully submitted,

Date: 9/14/98

By: 

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